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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/037,361	10/29/2001	James M. Byrd	5181-94400	6448

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Robert C. Kowert
Conley, Rose & Tayon, P.C.
P.O. Box 398
Austin, TX 78767

EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/037,361	Applicant(s) BYRD, JAMES M.	
	Examiner Dipakkumar Gandhi	Art Unit 2133	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 25 May 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 1-35.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Continuation of 11. does NOT place the application in condition for allowance because: Applicant's arguments filed on 5/25/2005 have been fully considered but they are not deemed to be persuasive.
Regarding claim 1, the applicant contends, " Kurihara does not disclose shifting a first bit having a different logical value than the same logical value across the initial data bit combination, wherein each time the first bit is shifted, one of n data bit combinations is generated."
The examiner disagrees and asserts that Kurihara teaches that according to this invention, in an error detection circuit which comprises a shift register having a plurality of storing stages which sequentially shifts input data and feeds back output data from an output stage to desired ones of the stages (fig. 2, col. 1, lines 44-48, Kurihara). Kurihara also teaches that when input data has entered from the input end, it is sequentially applied to the shift register portion 1 previously reset at "0" in all stages (col. 3, lines 13-15, Kurihara).

The applicant contends, " Kurihara does not teach generating one of n data bit combinations each time the first bit is shifted and providing each of the bit combinations to error detection/correction logic."
The examiner disagrees and asserts that Kurihara teaches that considering FIG. 2, the output from each stage of the shift register 101 is supplied to the parity generator 4, and a parity signal PARITY1 derived therefrom (fig. 2, col. 3, lines 66-68, Kurihara).

The applicant contends, "Kurihara is silent regarding the error detection/correction logic generating a set of check bits. Kurihara also does not disclose comparing the set of check bits generated by the error correction/detection logic with a known correct set of check bits for each of the n data bit combinations."
The examiner disagrees and asserts that Kurihara teaches an error detection circuit checking system for checking error detection within a data processing circuit (col. 4, lines 50-52, Kurihara). Kurihara teaches that a parity signal is generated from the parity generator in accordance with the data storing state of the shift register (col. 1, lines 49-51, Kurihara). Kurihara teaches that the parity signal derived from the parity generator is compared with the predicted parity signal in order to detect malfunction of the error detection circuit based on the result of the comparison (fig. 2, col. 1, lines 57-60, Kurihara).

The applicant contends, "Kurihara does not teach a comparison against a known correct set of check bits."
The examiner disgrees and asserts that Kurihara teaches that the parity prediction value is compared with the actual parity value applied from the parity generator 4 to the check circuit 5 (col. 3, lines 30-32, Kurihara).

Regarding claim 24, the applicant contends, "Kurihara fails to teach test check bit generating means for creating a set of test data bit combinations and providing the set of test data bit combinations to a check bit generator."
The examiner disagrees and asserts that Kurihara teaches that in an error detection circuit which comprises a shift register having a plurality of storing stages which sequentially shifts input data and feeds back output data from an output stage to desired ones of the stages, and a parity generator, and in which a parity signal is generated from the parity generator in accordance with the data storing state of the shift register (col. 1, lines 44-51, Kurihara).

The applicant contends, " Kurihara also fails to disclose wherein the set of test data bit combinations comprises n n-bit data bit combinations, wherein each possible value of each data bit is present in at least one of the n n-bit data bit combinations in the set of test data bit combinations. Kurihara fails to teach comparison means for comparing check bits output by the error/detection logic for each of the n n-bit data bit combinations in the set of test data bit combinatiions to known correct check bits for each of the n n-bit data bit combinations."
The examiner disagrees and asserts that Kurihara teaches that a parity predictive value of the shift register portion 1 of the nth term is calculated with the count values of the counters 3 and 2 and the zeroth P0 of a polynomial register, and the parity prediction value is compared with the actual parity value applied from the parity generator 4 to the check circuit 5. In the case where the values are not coincident with each other, an error signal is produced to take proper steps (fig. 2, col. 3, lines 27-34, Kurihara).

Regarding claim 27, the applicant contends, "Kurihara does not teach a method including providing a set of m+1 test code words to the error correction/detection logic, wherein each code word has m bits, wherein a first test code word in the set of m+1 test code words is a correct code word, wherein each test code word other than the first test code word comprises a single-bit error at a different bit position within the code word than each other test code word."
The examiner disagrees and asserts that Kurihara teaches an error detection circuit which comprises a shift register having a plurality of storing stages which sequentially shifts input data and feeds back output data from an output stage to desired ones of the stages, and a parity generator, and in which a parity signal is generated from the parity generator in accordance with the data storing state of the shift register (fig. 2, col. 1, lines 44-51, Kurihara). The examiner would like to point out that the error detection circuit in Kurihara detects a single bit error in a code word. The input data and the shift register provides the test code words to the error detection circuit.

Regarding claim 30, the applicant contends, "Kurihara does not teach a method including providing a set of test code words to the error correction/detection logic, wherein said providing comprises introducing an error into each of the test code words in the set by substituting check bits corresponding to an unused syndrome for a correct set of check bits within each test code word, wherein each test code word comprises substituted check bits corresponding to a different unused syndrome than each other test code word in the set of test code words."
The examiner disagrees and asserts that Arroyo teaches that an error detection and correction circuit is provided that periodically checks and corrects bit errors in the data words (col. 1, lines 36-38, Arroyo). Arroyo teaches a method comprising the steps of: supplying a first bit pattern to said ECC system, said first bit pattern including a plurality of bits each set to a logical state; generating first check bits at said ECC system based upon said first bit pattern; writing said first check bits to said memory; inducing an error by substituting second check bits for said first check bits when said first check bits are read from said memory; and comparing said first check bits with said second check bits to determine if said ECC system detected said error, wherein an error is detected when logical states of one or more corresponding bit positions within said first check bits and said second check bits differ (col. 9, lines 50-col. 10, line 9, Arroyo).

Regarding claim 34, the applicant contends, "Kurihara in view of Vishlitzky et al. does not teach providing each of a set of n data bit combinations to the error detection/correction logic. Kurihara fails to teach comparing the generated check bits with a known correct set of check bits for each input data bit combination. Vishlitzky et al fail to teach or suggest those limitations of claim 34 that are not taught by Kurihara."
The examiner disagrees and asserts that Kurihara teaches an error detection circuit which comprises a shift register having a plurality of storing stages which sequentially shifts input data and feeds back output data from an output stage to desired ones of the stages, and a parity generator, and in which a parity signal is generated from the parity generator in accordance with the data storing state of the shift register. The parity signal derived from the parity generator is compared with the predicted parity signal in order to detect malfunction of the error detection circuit based on the result of the comparison (col. 1, lines 44-51, lines 57-60, Kurihara).

Regarding claim 35, the applicant contends, "Kurihara in view of Arroyo fails to teach providing a subset of possible data bit combinations of n data bits to the error detection/correction logic, wherein the subset comprises n data bit combinations, wherein each possible value of each data bit is present in at least one of the n data bit combinations in the subset."
The examiner disagrees and asserts that Kurihara teaches an error detection circuit which comprises a shift register having a plurality of storing stages whtich sequentially shifts input data and feeds back output data from an output stage to desired ones of the stages, and a parity generator, and in which a parity signal is generated from the parity generator in accordance with the data storing state of the shift register (fig. 2, col. 1, lines 44-51, Kurihara). The examiner would like to mention that the input data and the shift register provides the n data bit combinations to the error correction/detection logic.

The applicant contends, "Kurihara in view of Arroyo fails to teach verifyin the error detection/correction logic by comparing a set of check bits generated by the error detection/correction logic for each of the n data bit combinations in the subset with a set of known correct check bits."
The examiner disagrees and asserts that Kurihara teaches comparing the preditecd value with the value actually generated from the error correction circuit, in order to detect malfunction of the error detection circuit (figure 1, 2, col. 2, lines 65-68, Kurihara). Kurihara teaches that a parity predictive value of the shift register portion 1 of the nth term is calculated with the count values of the counters 3 and 2 and the zeroth Po of a polynomial register, and the parity prediction value is compared with the actual parity value applied from the parity generator 4 to the check circuit 5. In the case where the values are not coincident with each other, an error signal is produced to take proper steps (fig. 2, col. 3, lines 27-34, Kurihara).

The applicant contends, " Kurihara in view of Arroyo also fails to teach providing a first set of m+1 test code words to the error detection/correction logic, wherein a first test code word is a correct test code word and where each other test code word in the set of m+1 test code words comprises a single-bit error, wherein each test code word having a single-bit error has the single-bit error at a different bit position than each other test code word that has a single-bit error."
The examiner disagrees and asserts that Arroyo teaches that an error detection and correction circuit is also provided that periodically checks and corrects bit errors in the data words (col. 1, lines 36-38, Arroyo). Arroyo also teaches that in the event that an error condition for a single bit data error is detected, the ECC correction logic is utilized to correct the invalid data bit (col. 1, lines 25-27, Arroyo). Arroyo teaches that at step 14 it is then determined that if each data address in the verified memory section has been tested. Different data addresses are used in the present invention so that all of the ECC logic in memory control chip 3 is tested. If the test is not complete, the process continues to step 15 wherein the CPU increments the data value by walking a bit through each position, thereby changing the ECC code generated by logic 31. The process then returns to step 5. Once all of the memory section is tested, the multiplexer 33 is disabled at step 15a (col. 6, line 61 to col. 7, line 3, Arroyo).

The applicant contends, "Kurihara in view of Arroyo also fails to teach providing a second set of test code words to the error detection / correction logic, wherein each test code word in the second set comprises an error introduced by substituting check bits corresponding to an unused syndrome for a correct set of check bits within a correct code word, wherein each test code word in the second set comprises substituted check bits corresponding to a different unused syndrome than each other test code word in the second set of test code words."
The examiner disagrees and asserts that Arroyo teaches that an error detection and correction circuit is also provided that periodically checks and corrects bit errors in the data words (col. 1, lines 36-38, Arroyo). Arroyo teaches that these ECC check bits corresponding to the generated data are then written to memory 5 from bus 4. Thus, at step 4, the actual test data from CPU 1 is written to memory 5 along with corresponding ECC check bits generated by logic 31. The 64 bit data and 8 bit ECC check bits are then read from the verified section of memory 5 at step 5. At this time, the 8 bit logical zeros are forced through enabled multiplexer 43 and to comparator 45. Additionally, logic 41 generates ECC check bits based on the actual data, which is being read from memroy 5 on bus 10. Therefore, the ECC check bits actually corresponding to data on bus 10 and the 8 bit logical zero check bits are both provided to comparator 45, which then performs a comparison and generates a syndrome, at step 6. Additionally, at step 6, the status and address registers are written with the type of error, syndrome and location of the error. It can be seen that an error will in face occur because the check bits generated by logic 41 arew based upon actual data while 8 bits of logical zeros have been substituted for the check bits generated by logic 31 and input to comparator 45. At step 7 it is then determined if a single bit error has occurred and if so the process continues to step 8 where logic 47 receives the check bits (col. 7, lines 22-44, Arroyo).

Regarding claim 13, the applicant contends, "Kurihara in view of Fielder fails to teach a computer readable medium comprising program instructions computer executable to: create and initial data bit combination having n bits, wherein each data bit in the initial data bit combination has a same logical value as each other data bit in the initial data bit combinatiion; shift a first bit having a different logical value than the same logical value across the initial data bit combination, wherein each time the first bit is shifted, one of n data bit combinations is generated; provide each of the n data bit combinations to error detection/correction logic; compare a set of check bits generated by the error correction/detection logic with a known correct set of check bits for each of the n data bit combinations; and dependent on an outcome of said comparing, generate an indication of whether the error detection/correction logic correctly generated the set of check bits."
The examiner would like to point out that the remarks above regarding claim 1 in view of Kurihara also apply here to claim 13.

Additionally the applicant contends, "Fielder et al. reference is not analogous art."
The examiner disagrees and asserts that Fielder et al. teach a program of instructions executable by a machine, such as a programmable digital signal

processor or computer processor, to perform such a process can be conveyed by a medium readable by the machine, and the machine can read the medium to obtain the program and responsive thereto perform such process (col. 4, lines 60-64, Fielder et al.).
Fielder et al. also teach that preferred embodiments use program-controlled processors, such as those in the DSP563xx line of digital signal processors from Motorola. Programs for such implementatiions may include instructions conveyed by machine readable media, such as baseband or modulated communication paths and storage media (col. 3, lines 4-9, Fielder et al.).Fielder et al. teach that a processing system for a standard data channel includes a memory unit and a program-controlled processor (col. 3, lines 52-54, Fielder et al.).
Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kurihara's patent with the teachings of Fielder et al. by including an additional step of using a computer readable medium comprising program instructions that are computer-executable.

Claim Rejections - 35 USC 102:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 3-5, 24, 25, 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurihara (US 4,107,649). Please see the office action mailed on 07/28/2004 for details.

2. Claim 30 is rejected under 35 U.S.C. 102(b) as being anticipated by Arroyo et al. (US 5,502,732). Please see the office action mailed on 07/28/2004 for details.

Claim Rejections - 35 USC 103:

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 2 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Kurihara (US 4,107,649) in view of Nielson et al. (US 5,619,642). Please see the office action mailed on 07/28/2004 for details.

4. Claims 6-12, 26, 31-33, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) as applied to claim 3 above, and further in view of Arroyo et al. (US 5,502, 732). Please see the office action mailed on 07/28/2004 for details.

5. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) in view of Fielder et al. (US 6,446,037 B1). Please see the office action mailed on 07/28/2004 for details.

6. Claims 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) and Fielder et al. (US 6,446,037 B1) as applied to claim 14 above, and further in view of Arroyo et al. (US 5,502, 732). Please see the office action mailed on 07/28/2004 for details.

7. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) in view of Vishlitzky et al. (US 5,809,332). Please see the office action mailed on 03/21/2005 for details.